What is claimed is:

1. A method to polish down conductive lines in the manufacture of an integrated circuit device, said method comprising:

providing a plurality of conductive lines overlying a substrate;

depositing a high density plasma (HDP) oxide layer overlying said substrate and said conductive lines wherein, in the regions between said conductive lines, first planar surfaces of said HDP oxide layer are formed below the top of said conductive lines;

sputtering down said HDP oxide layer overlying said conductive lines such that second planar surfaces of said HDP oxide layer are formed above said conductive lines;

thereafter depositing a polish stopping layer overlying said HDP oxide layer;

depositing a film layer overlying said polish stopping layer;

polishing down said film layer to said polish stopping layer overlying said second planar top surfaces; and

polishing down said film layer, said polish stopping layer, and said conductive lines to said polish stopping layer overlying said first planar top surfaces to complete said polishing down of said conductive lines.

2. The method according to Claim 1 further comprising depositing a conformal oxide layer overlying said plurality of conductive lines prior to said step of depositing a high density plasma (HDP) oxide layer overlying said substrate and said conductive lines.

3. The method according to Claim 1 wherein said conductive lines comprise polysilicon lines.

4. The method according to Claim 1 wherein said conductive lines comprise n-type polysilicon and further comprising the steps of:

forming an oxide layer overlying said conductive lines after said step of polishing down said film layer, said polishing stop layer, and said conductive lines;

depositing a p-type polysilicon layer overlying said oxide layer; and

patterning said p-type polysilicon layer to form p type polysilicon lines that cross over said conductive lines with said oxide layer therebetween.

5. The method according to Claim 4 wherein said conductive lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile memory device.

6.The method according to Claim 5 wherein other said conductive lines are not bit lines but are used to provide a uniform pattern density of said conductive lines across said substrate.

7. The method according to Claim 1 wherein said step of sputtering down said HDP oxide layer comprises bombardment with argon ions.

8. The method according to Claim 1 wherein said film layer comprises silicon oxide and said polish stopping layer comprises silicon nitride.

9. The method according to Claim 8 wherein said film layer comprises high density plasma (HDP) oxide.

10. The method according to Claim 8 wherein said film layer comprises chemical vapor deposited (CVD) oxide.

11. A method to polish down polysilicon lines in the manufacture of an integrated circuit device, said method comprising:

providing a plurality of polysilicon lines overlying a

substrate;

depositing a high density plasma (HDP) oxide layer overlying said substrate and said polysilicon lines wherein, in the regions between said polysilicon lines, first planar surfaces of said HDP oxide layer are formed below the top of said polysilicon lines;

sputtering down said HDP oxide layer overlying said polysilicon lines such that second planar surfaces of said HDP oxide layer are formed above said polysilicon lines;

thereafter depositing a polish stopping layer overlying said HDP oxide layer;

depositing a film layer overlying said polish stopping layer;

polishing down said film layer to said polish stopping layer overlying said second planar top surfaces; and

polishing down said film layer, said polish stopping layer, and said polysilicon lines to said polish stopping layer overlying said first planar top surfaces to complete said polishing down of said polysilicon lines.

12. The method according to Claim 11 wherein said polysilicon lines comprise n-type polysilicon and further comprising the steps of:

forming an oxide layer overlying said polysilicon

lines after said step of polishing down said film layer, said polishing stop layer, and said polysilicon lines;

depositing a p-type polysilicon layer overlying said oxide layer; and

patterning said p-type polysilicon layer to form p type polysilicon lines that cross over said n-type polysilicon lines with said oxide layer therebetween.

13. The method according to Claim 12 wherein said n-type polysilicon lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile memory device.

14. The method according to Claim 13 wherein other said n-type polysilicon lines are not bit lines but are used to provide a uniform pattern density of said polysilicon lines across said substrate.

15. The method according to Claim 11 wherein said polysilicon lines further comprise a stack of a second polysilicon layer overlying a first polysilicon layer with a metal silicide layer therebetween.

16. The method according to Claim 11 wherein said step of sputtering down said HDP oxide layer comprises bombardment with argon ions.

17. The method according to Claim 11 wherein said film layer comprises silicon oxide and said polish stopping layer comprises silicon nitride.

18. The method according to Claim 17 wherein said film layer is high density plasma (HDP) oxide CVD oxide.

19. A method to form anti-fuse memory devices in the manufacture of an integrated circuit device, said method comprising:

providing a plurality of n-type polysilicon lines overlying a substrate;

depositing a high density plasma (HDP) oxide layer overlying said substrate and said n-type polysilicon lines wherein, in the regions between said n-type polysilicon lines, first planar surfaces of said HDP oxide layer are formed below the top of said n-type polysilicon lines;

sputtering down said HDP oxide layer overlying said n-type polysilicon lines such that second planar surfaces of

said HDP oxide layer are formed above said n-type polysilicon lines;

thereafter depositing a polish stopping layer overlying said HDP oxide layer;

depositing a film layer overlying said polish stopping layer;

polishing down said film layer to said polish stopping layer overlying said second planar top surfaces;

polishing down said film layer, said polish stopping layer, and said n-type polysilicon lines to said polish stopping layer overlying said first planar top surfaces to complete said polishing down of said n-type polysilicon lines;

forming a dielectric layer overlying said n-type polysilicon lines;

depositing a p-type polysilicon layer overlying said dielectric layer; and

patterning said p-type polysilicon layer to form p-type polysilicon lines that cross over said n-type polysilicon lines with said oxide layer therebetween to thereby complete said anti-fuse memory devices.

20. The method according to Claim 19 wherein said n-type

polysilicon lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile memory device.

21. The method according to Claim 19 wherein other said n-type polysilicon lines are not bit lines but are used to provide a uniform pattern density of said n-type polysilicon lines across said substrate.

22.The method according to Claim 19 wherein said polysilicon lines further comprise a stack of a second polysilicon layer overlying a first polysilicon layer with a metal silicide layer therebetween.

23. The method according to Claim 19 wherein said step of sputtering down said HDP oxide layer comprises bombardment with argon ions.

24.The method according to Claim 19 wherein said dielectric layer comprises silicon oxide or silicon nitride.

25. The method according to Claim 19 wherein said film layer comprises silicon oxide and said polish stopping layer comprises silicon nitride.

26. The method according to Claim 25 wherein said film layer comprises high density plasma (HDP) oxide.

27. The method according to Claim 25 wherein said film layer comprises chemical vapor deposited (CVD) oxide.

28. An integrated circuit device, said device comprising:

a plurality of conductive lines overlying a substrate;

a liner oxide layer disposed conformally on the sidewalls of said conductive line; and

a HDP oxide layer overlying said substrate in regions between said liner oxide layer.

29. The device according to Claim 28 wherein said conductive lines comprise polysilicon.

30. The device according to Claim 28 wherein said conductive lines comprise bit lines and word lines for a nonvolatile memory device.

31. The device according to Claim 28 further comprising a polish stopping layer overlying said HDP oxide layer wherein the top surfaces of said polish stopping layer are approximately at the same height as the top surfaces of

said conductive lines and wherein said polish stopping layer does not overlie said conductive lines.

32. An integrated circuit device, said device comprising:

a plurality of conductive lines overlying a substrate;

a liner oxide layer disposed conformally on the sidewalls of said conductive line;

a HDP oxide layer overlying said substrate in regions between said liner oxide layer; and

a polish stopping layer overlying said HDP oxide layer wherein the top surfaces of said polish stopping layer are approximately at the same height as the top surfaces of said conductive lines and wherein said polish stopping layer does not overlie said conductive lines.

33. The device according to Claim 32 wherein said conductive lines comprise polysilicon.

34. The device according to Claim 32 wherein said conductive lines comprise bit lines and word lines for a nonvolatile memory device.

35. An integrated circuit device, said device comprising:

a plurality of polysilicon lines overlying a substrate;

a high density plasma (HDP) oxide layer overlying said substrate in the regions between said polysilicon lines; and

a polish stopping layer overlying said HDP oxide layer wherein the top surfaces of said polish stopping layer are approximately at the same height as the top surfaces of said polysilicon lines and wherein said polish stopping layer does not overlie said polysilicon lines.

36. The device according to Claim 35 wherein said polysilicon lines comprise n-type polysilicon and further comprising the features of:

a dielectric layer overlying said n-type polysilicon lines; and

p-type polysilicon lines overlying said oxide layer wherein said p-type polysilicon lines cross over said n-type polysilicon lines with said dielectric layer therebetween.

37. The device according to Claim 36 wherein said dielectric layer comprises silicon oxide or silicon nitride.

38. The device according to Claim 35 wherein said n-type polysilicon lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile memory device.

39. The device according to Claim 35 wherein other said n-type polysilicon lines are not bit lines but are used to provide a uniform pattern density of said n-type polysilicon lines across said substrate.

40. The device according to Claim 35 wherein said polysilicon lines further comprise a stack of a second polysilicon layer overlying a first polysilicon layer with a metal silicide layer therebetween.

41. The device according to Claim 35 wherein said polish stopping layer comprises silicon nitride.